

FIG. 1A

FIG. 1B



**FIG. 3**

Functional Unit

1 2 3 4

406

stage 1

stage 2

408

stage 3

stage 4

402

404

Cycle Actual Executed Code

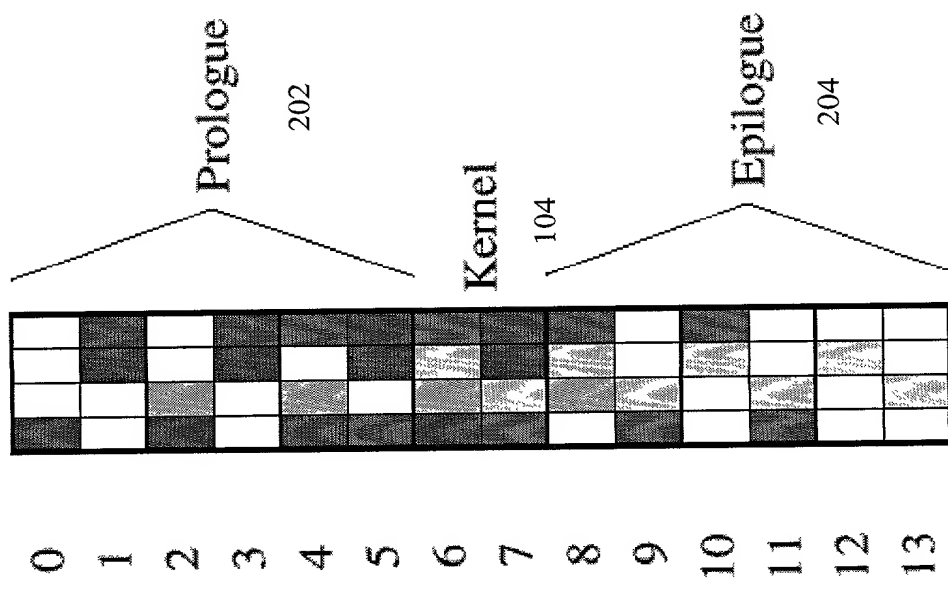


FIG. 4B

FIG. 4A



**FIG. 5**

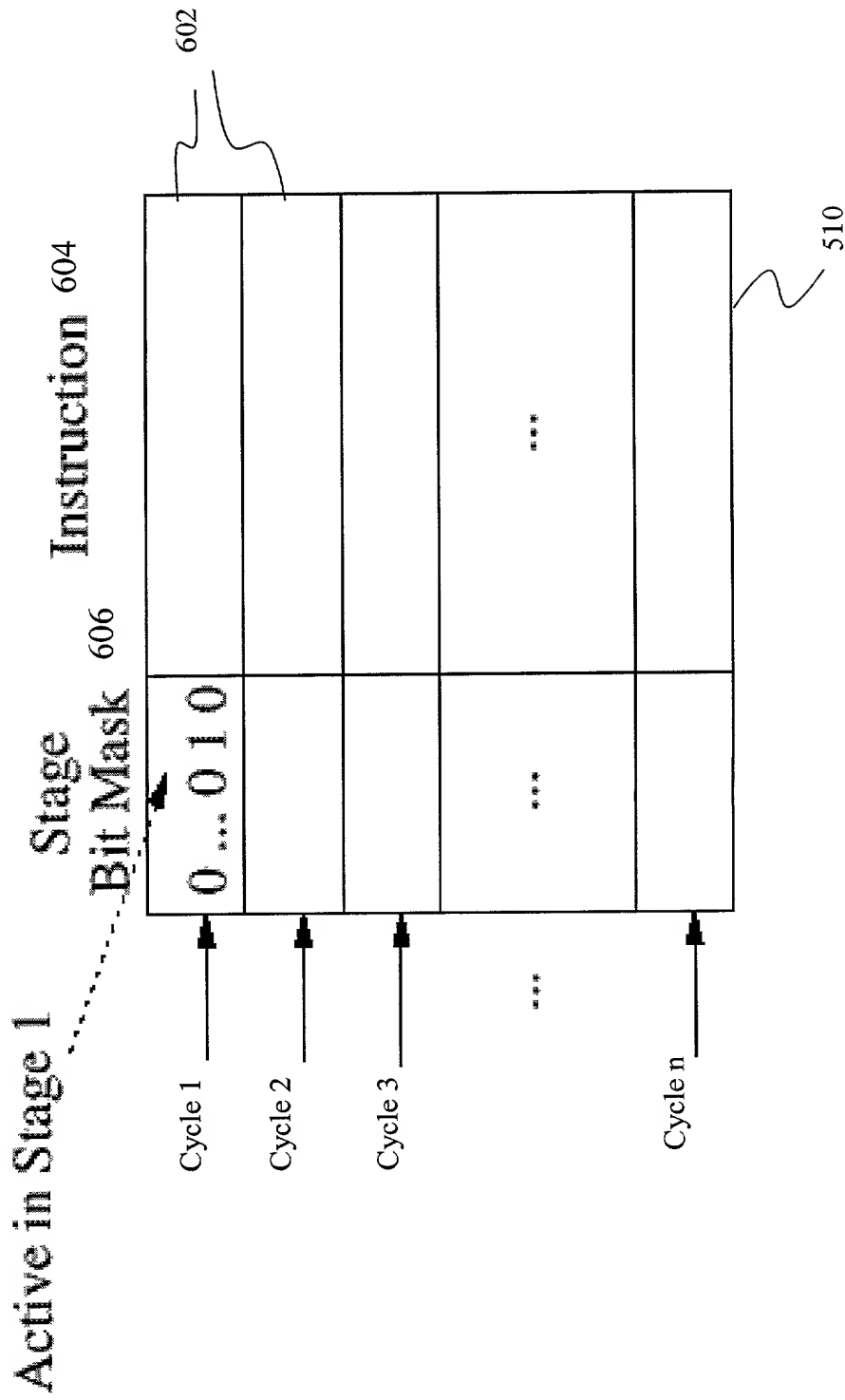


FIG. 6

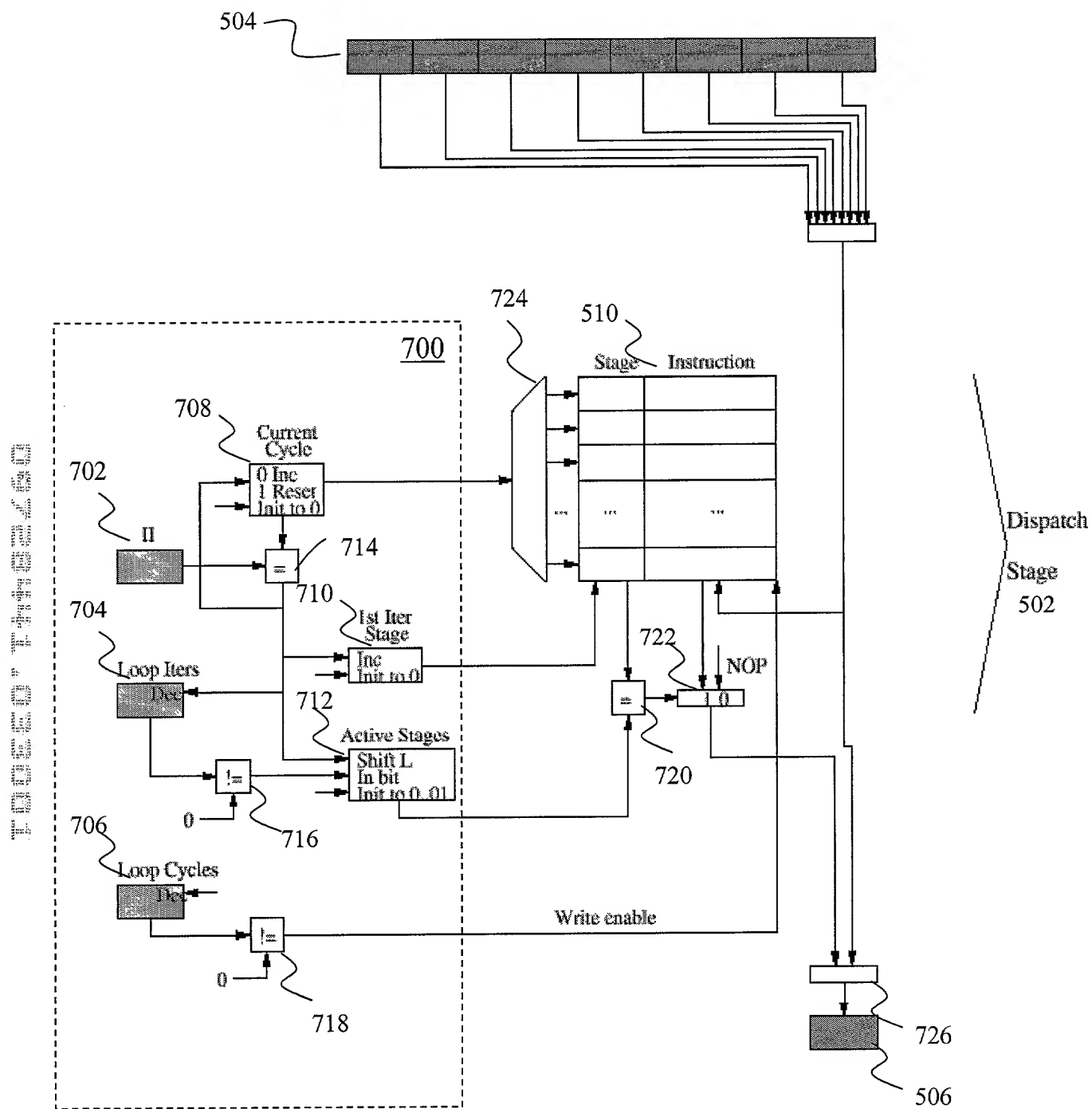


FIG. 7

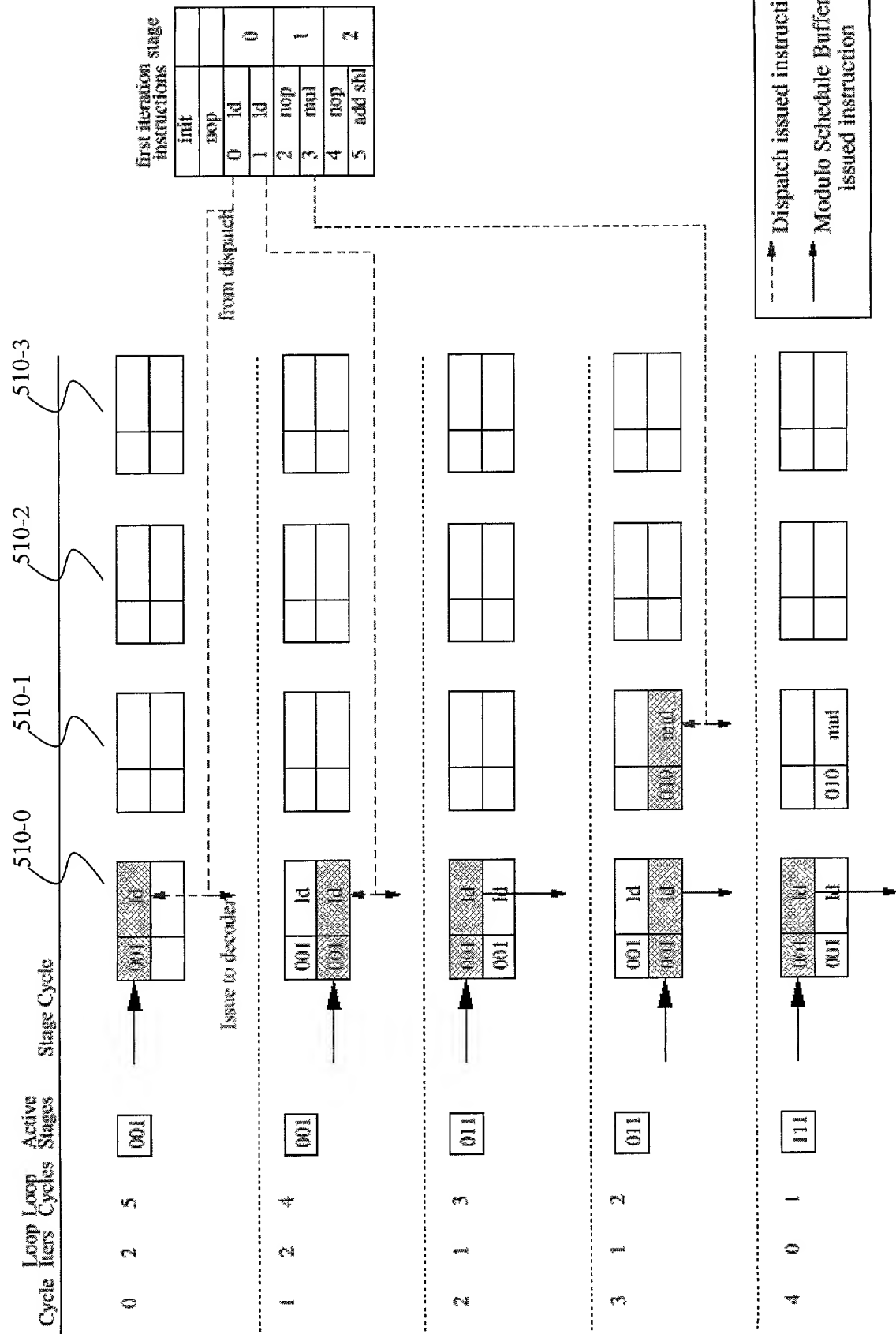


FIG. 8A

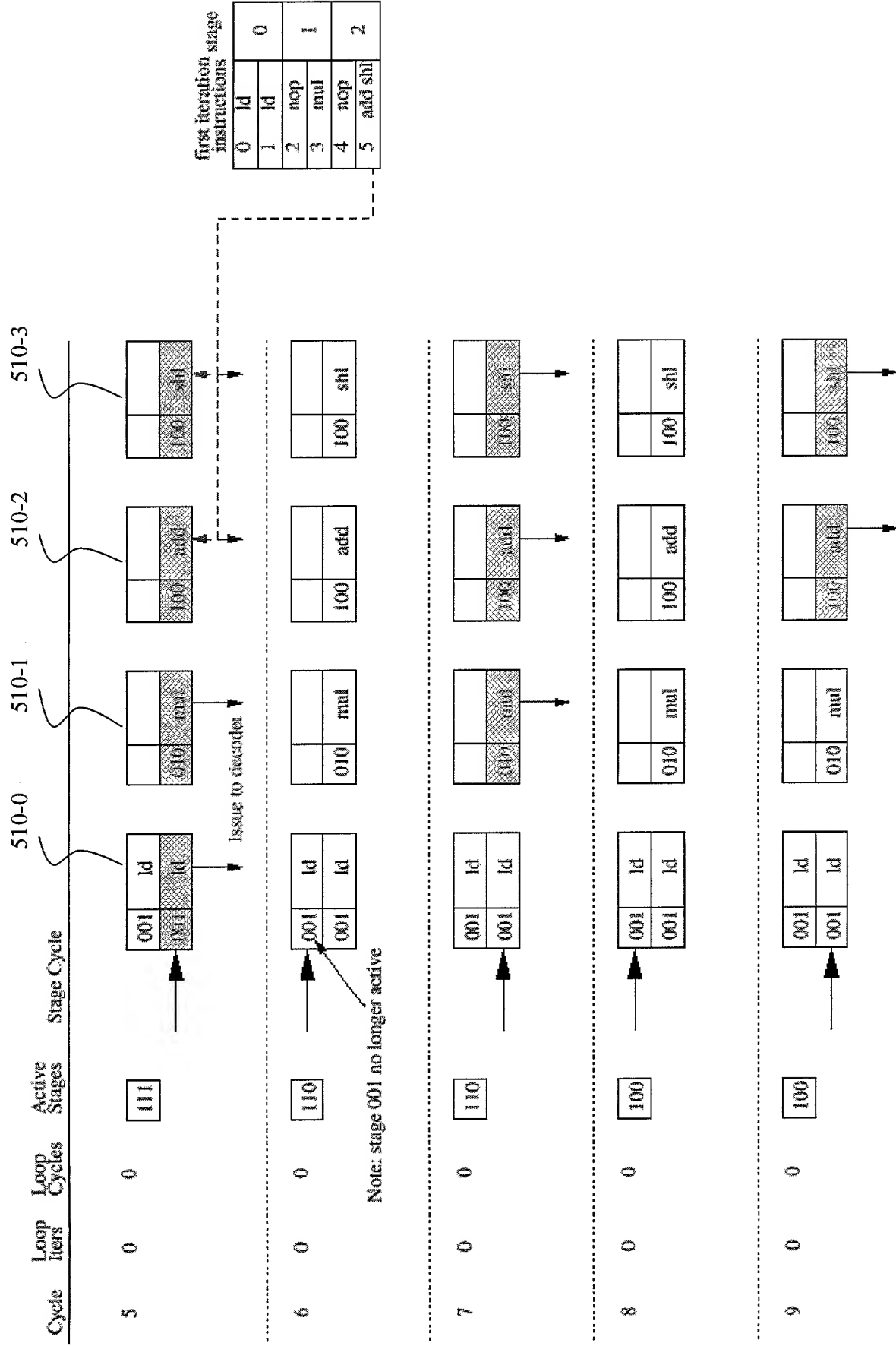


FIG 8B



cycle	RTL	inst.	latency
0	$r1 \leftarrow 0$		
1	$r1 \leftarrow r1 * 5$	mul	3
2	$r1 \leftarrow r1 + 4$	add	1
3	st [r2], r1		
4	st [r3], r1		

FIG. 9

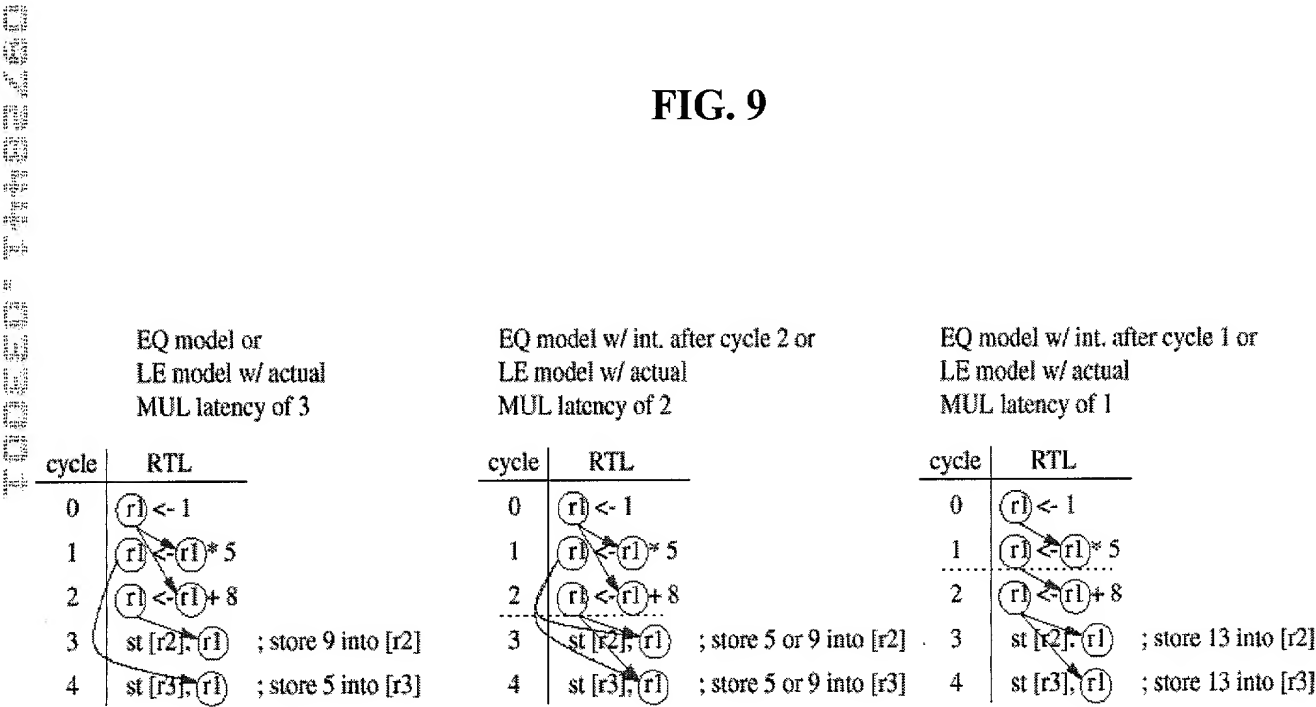
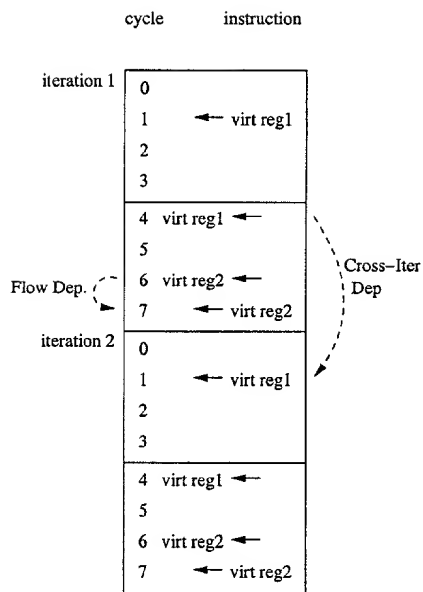
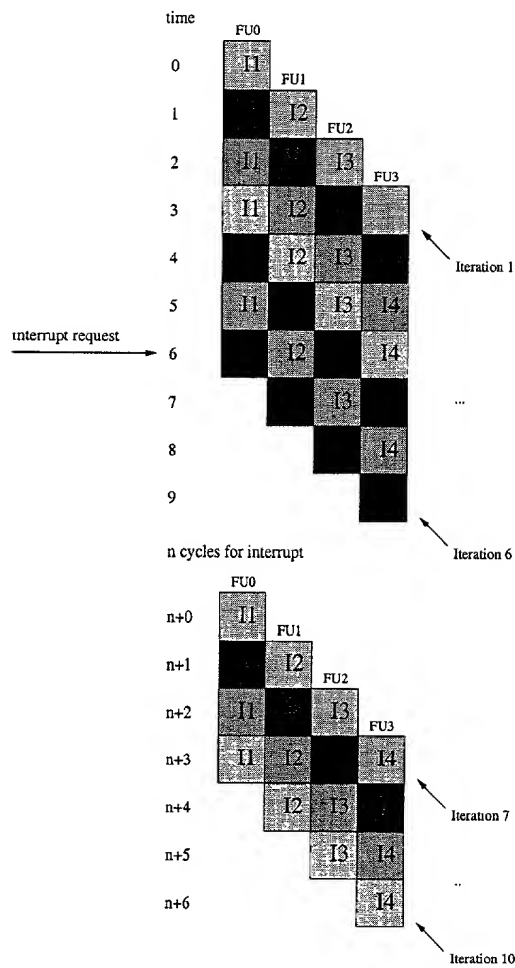


FIG. 10A

FIG. 10B

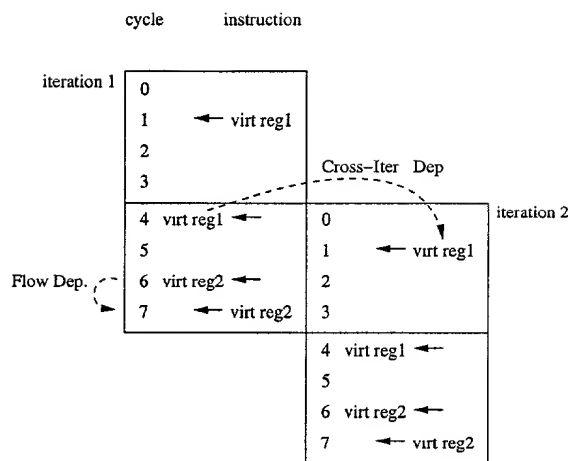
FIG. 10C

FIG. 11



(a) Traditional register allocation of the loop body.

FIG. 12A



(b) Modulo schedule-aware register allocation of the loop body.

FIG. 12B

